

## Abstract of the Disclosure

A method and apparatus for testing a processor is described. In one embodiment, a NOP  
PSR generates error checking NOP instructions during a pipeline stall. The insertion of these  
numerous NOP instructions ensure the fact that the checking hardware checks more frequently  
5 and has more locations to check. Also, taking advantage of modern processor optimizations for  
handling NOPs minimizes any impact on processor performance.

0975131-123000